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Shanghai Silicon Intellectual Property Exchange Co.,

Overview

Shanghai Silicon Intellectual Property Exchange Co., Ltd. (SSIPEX) founded in 2003, is one of the earliest IP exchange platform in the world. SSIPEX is one of main sponsors for Integrated circuit IP core transfer specification series standards in China. SSIPEX has excellent IC design facilities, IP information analysis & management system. We provide IP/SoC design service, test and verification, IP core trade and exchange, IP training and IP forensic service, etc.
SSIPEX handles various types of IPs, including Renesas.

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HARDWARE IP TECHNOLOGY MAP FOR IP LICENSE PRODUCTS

Hardware IP can be provided are as shown in the table below. Please contact us for IPs not listed.

Category	IP	Protocols	Up to	TSMC 40LP/ULP	TSMC 28HPC	TSMC 28HPC+	TSMC 16FFC	TSMC 12FFC	TSMC N7/N7+	UMC 28HPC+	Samsung 28FDSOI	Samsung 7LPP
Interface(PHY)	32G SerDes	PCIe5/4/3/2/1, 10G-KR	32G					✔	✔			
	16G SerDes	PCIe4/3/2/1, 10G-KR	16G		●	○	○	○				
	10G SerDes	PCIe3/2/1, 10G-KR	10G			●						
	5G SerDes	PCIe2/1, QSGMII	5G		●	●		●				
	USB3.1		10G		●							
	USB3.0		5G		●	●		●				
	USB2.0		480Mbps	●	●	●				●	○	
	USB1.1		12Mbps	●							●	
	SATA3		6G		●	●		○				
	MIPI D-PHY TX	DSI-2 1.1	1G									
	MIPI D-PHY RX	CSI-2 2.1	1G	●								
	SGMII		1.25G			●						
	FPD-Link		1G	●		●						
	LVDS (ANSI644, IEEE1596)	MSC, RSDS, MLB, CCP2, etc	1G	●	●	●	●	○	○			
Analog IP	PLL			●	●	●	●	○	○			
	ADC			●	●	●	✔	✔	✔			
	DAC			●	✔	✔	✔	✔	✔			
	Temp. Sensor			●		●	○	○				
Memory IP	SRAM			●	●	●	●	●	○	●	●	
	TCAM				●	●	●	●	○	●		
Fundamental IP	Standard Cell			●		●						
	GPIO			●	●	●	●					

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● Ready for MP ○ In development ✔In planning

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IP LICENSE PRODUCTS LINE UP OVERVIEW

FOR PROVIDING TOTAL SOLUTIONS AT SEMICONDUCTOR PRODUCT

- Lineup around 80 IP licensed products (including to be released soon), is expanding continuously.
- ~~Considering advanc~~ed IP development in response to market demands, so please give us your needs.

Processor IP (Subsystem)	Digital IP	Interface IP	Memory IP	Analog IP	Other IP
RX	GTP (General Purpose Timer)	Ethernet TSN	40/28/16/12/7nm SRAM	16nm 4.1G PLL	16nm GPIO
SH-4A	SCI	Ethernet AVB	28/16/12/7nm TCAM	Multiplying PLL	28nm GPIO
SH-4	SPI	USB 2.0		SSCG PLL	Standard cell
SH3-DSP	I3C	SATA 3.2		Deskew PLL	
SH-2A	I2C	PCIe-Gen4		Fractional PLL	
SH2-DSP		FPD-Link		R-2R DAC	
H8S		MIPI		R-String DAC	
M32R		CAN FD		SAR ADC	
		CAN		Temp. Sensor	
		SerDes PHY			
8 IPs	**5** IPs	**30** IPs	**9** IPs	**24** IPs	**5** IPs

MBD
Motor timer
Multicore PILS

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MEMORY CORE — SRAM&TCAM IP LINEUP OVERVIEW

The lineup overview of SRAM and TCAM cores, which aligned Foundry/Process Node, is in the table below.

Foundry	Node	Cell Type	Port Type							
			1WR	2CLK		1CLK			TCAM	1WR 1.8-3.3V
				1W1R	2WR	1W1R	2WR	2W2R		
TSMC	40LP	-	✓	✓	✓					✓
	28HPL	-	✓		✓	✓				
	28 HPC	LL	✓	✓	✓	✓		✓		
		GL							✓	
	28 HPC+	ULL	✓	✓	✓	✓	✓	✓	✓	
		GL	✓	✓	✓	✓	✓	✓	✓	
	16FF+	LL	✓	✓	✓	✓				
	16FFC	LL	✓	✓	✓	✓			✓	
	12FFC	LL	✓	✓	✓	✓			✓	
	7FF	-	✓	✓					✓	
Samsung	7LPP	LPP	TBD	TBD	TBD				TBD	

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INTERFACE CORES（LINK）

The Interface Link cores can be provided are as shown in the table below

Function	IP name	Process (or Soft macro)	Status	Document	Inquiry
USB LINK	**USB3.1 (Gen1) xHCI Host Controller**	Soft macro	Preliminary (Inquiry required)	IP_Datasheet(I-15):USB3.1 Gen1 xHCI Host Controller IP Core (PDF)	CONTACT
	USB3.1 (Gen1) Peripheral Controller	Soft macro	Preliminary (Inquiry required)	IP_Datasheet(I-16):uu3pcss/uu3pcssaxi (PDF)	
	USB2.0 EHCI Host Controller	Soft macro	Available	IP_Datasheet(I-12):uu2hcahbutmi (PDF)	
	USB2.0 On-The-Go (OTG) Controller	Soft macro	Available	IP_Datasheet(I-13):uu2otgahbutmi (renesas.com)	
	USB2.0 Peripheral Controller	Soft macro	Available	IP_Datasheet(I-14):uu2pcahbutmi (renesas.com)	
PCI Express LINK	**Configurable PCI Express 4.0 Link Controller**	Soft macro	Preliminary (Inquiry required)	IP_Datasheet(I-22):Configurable PCI Express 4.0 Link Controller (PDF) Simulation	CONTACT
SATA LINK	**SATA3.2 Host Controller**	Soft macro	Preliminary (Inquiry required)	P_Datasheet(I-17):Serial ATA 3.2 Host Link/Transport IP Core (PDF)	CONTACT
CAN	**CAN controller**	Soft macro	Preliminary (Inquiry required)	IP_Datasheet(D-4):CAN (PDF)	CONTACT
CAN FD	**CAN FD controller (Multi channel version)**	Soft macro	Preliminary (Inquiry required)	IP_Datasheet(I-23):CAN FD controller (PDF)	CONTACT
CAN FD Lite	**CAN FD controller (Single channel version)**	Soft macro	Available	IP_Leaflet_CAN_FD_LITE (renesas.com)	CONTACT
Ethernet AVB	**Ethernet AVB End Station**	Soft macro	Preliminary (Inquiry required)	IP_Datasheet(I-29):Ethernet AVB (PDF)	CONTACT
Ethernet TSN	**Ethernet TSN End Station**	Soft macro	Preliminary (Inquiry required)	IP_Datasheet(I-24):EthernetTSN End Station (PDF) Application example	CONTACT
	Ethernet TSN Layer 2 Switch	Soft macro	Preliminary (Inquiry required)	IP_Datasheet(I-25):Ethernet TSN Layer 2 Switch (PDF) Application example	

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INTERFACE CORES（PHY）-1

The Interface PHY cores can be provided are as shown in the table below

Function	IP name	Process (or Soft macro)	Status	Document	Inquiry
PCIe/USB/SATA PHY Appilcation example	**Combo SerDes PHY SerDes (PCIe/USB/SATA)**	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-1):Combo Serdes PHY for TSMC 28nm HPM (renesas.com)	**CONTACT**
	Combo PHY PIPE + SerDes (PCIe/USB/SATA)	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-2):Combo PHY for TSMC 28nm HPM (renesas.com)	
	SerDes PHY upto 10Gbps (PCIe gen3, 10GKR, SATA3)	Soft macro & TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-3):16Gpbs SerDes for TSMC 28nm HPC+ (renesas.com)	
	SerDes PHY upto 16Gbps (PCIe gen4, 10GKR, SATA3)	Soft macro & TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-4):16Gpbs SerDes for TSMC 28nm HPC (renesas.com)	
	PCIe2/USB3SS Combo PHY (SandyMLS+ 5GSerDes PHY)	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-5):SerDes PHY for TSMC 28nm HPC+ (renesas.com)	
	SATA3 PHY (SandyMLS+ 6GSerDes PHY)	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-6):SATA PHY for TSMC 28nm HPC+ (renesas.com)	
	USB2.0 MultiPort PHY: UTMI+ Level3 Multiport Transceiver	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-10):USB2.0 Transceiver for TSMC 28nm HPC+ (renesas.com)	
	USB2.0 MultiPort PHY: UTMI+ Level3 Multiport Transceiver	Samsung 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-26):USB2.0 Transceiver for Samsung 28nm (renesas.com)	
	USB2.0 PHY: UTMI+ Level3 Transceiver	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(I-9):USB2.0 Transceiver for TSMC 40nm LP (renesas.com)	
	USB2.0 Full Speed (FS) Transceiver	TSMC40nm, Samsung 28nm	Preliminary (Inquiry required)	IP_Leaflet:USB2.0 FS Transceiver for TSMC 40nm LP (renesas.com)	

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INTERFACE CORES（PHY）-2

The Interface PHY cores can be provided are as shown in the table below

Function	IP name	Process (or Soft macro)	Status	Document	Inquiry
FPD-Link	**FPD-Link RX**	Soft macro & TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-19):FPD-Link Receiver for TSMC 28nm HPC+ (PDF)	**CONTACT**
	FPD-Link TX	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-20):FPD-Link Transmitter for TSMC 28nm HPC (PDF)	
LVDS	**LVDS IO Buffer**	TSMC16nm, 28nm, 40nm	Preliminary (Inquiry required)	IP_Leaflet:LVDS IO Buffer (renesas.com)	**CONTACT**
MIPI	**MIPI D-PHY CSI**	Soft macro & TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(I-18):MIPI D-PHY Receiver for TSMC 40nm LP (PDF)	**CONTACT**
	MIPI D-PHY CSI/DSI	Soft macro & TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(I-27):MIPI D-PHY Tx/Rx for TSMC 40nm LP (PDF)	
	MIPI D-PHY CSI/DSI	Soft macro & Samsung 28nm	Preliminary (Inquiry required)	IP_Datasheet(I-28):MIPI D-PHY Tx/Rx for Samsung 28nm (PDF)	

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ANALOG CORES -CLOCK

The Clock cores can be provided are as shown in the table below

Function	IP name	Process (or Soft macro)	Status	Document	Inquiry
Clock	**4.1GHz Multiplying PLL**	TSMC 16nm	Preliminary (Inquiry required)	IP_Datasheet(A-24):Analog-PLL For Frequency Multiplying (PDF)	CONTACT
	4GHz Fractional PLL	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-7):Analog-PLL For Fractional Multiplying (PDF)	
	1.8GHz SSCG PLL (HPC+)	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-8):Analog-PLL For Spread Spectrum Clock (PDF)	
	1.4GHz Deskew PLL	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-9):Analog-PLL For Skew adjust (PDF)	
	7. GHz Multiplying PLL	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-3):Analog-PLL For Frequency Multiplying (PDF)	
	5GHz Multiplying PLL	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-4):Analog-PLL For Frequency Multiplying (PDF)	
	8. GHz SSCG PLL (HPM/HPC)	TSMC 28nm	Preliminary (Inquiry required)	P_Datasheet(A-5):Analog-PLL For Spread Spectrum Clock (PDF)	
	1.68GHz Deskew PLL	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-6):Analog-PLL For Skew adjust (PDF)	
	1.25GHz Multiplying PLL	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-1):Analog-PLL For Frequency Multiplying (PDF)	
	1.056GHz SSCG PLL	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-2):Analog-PLL For Spread Spectrum Clock (PDF)	

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ANALOG CORES -CONVERTOR

The Convertor cores can be provided are as shown in the table below

Function	IP name	Process (or Soft macro)	Status	Document	Inquiry
Convertor	**2ch 12-bit R-2R DAC w/ buffer (3us)**	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-10):Single/Dual Channel 12b D/A Converter (PDF)	CONTACT
	2ch 8-bit R-String DAC (2uA)	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-11):Dual Channel 8b D/A Converter (PDF)	
	12-bit SAR ADC (1.8V, 0.5us) Process : TSMC CLN28HPM/HPC Available metallization technologies :4X2Y2R+AP RDL	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-12):12bit 2MSps SAR ADC (PDF)	
	12-bit SAR ADC (1.8V, 0.5us) Process : TSMC CLN28HPC+ Available metallization technologies :5X2Y2R_UT+AP RDL	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-13):12bit 2MSps SAR ADC (PDF)	
	12-bit SAR ADC (3V, 0.4us) Process : TSMC CLN40LP Available metallization technologies :4X2Y1Z+AP	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-14):12bit 2.5MSps SAR ADC (PDF)	
	12-bit SAR ADC (3V, 0.4us) Process : TSMC CLN40LP Available metallization technologies :4X2Z+AP	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-15):12bit 2.5MSps SAR ADC (PDF)	

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ANALOG CORES –TEMP. SENSOR

The Temperature Sensor cores and analog elements can be provided are as shown in the table below

Function	IP name	Process (or Soft macro)	Status	Document	Inquiry
Temp. Sensor, etc	**Temp. Sensor (with ADC)**	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-17):Temperature Sensor IP (PDF)	**CONTACT**
	Temp. Sensor (with analog output buffer)	TSMC 28nm	Preliminary (Inquiry required)	IP_Datasheet(A-18):Temperature Sensor IP (PDF)	
	Temp. Sensor (with analog output buffer)	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-16):Temperature Sensor IP (PDF)	
	Voltage Detector (3ch)	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-19):Voltage Detector (3ch) (PDF)	
	High Speed Comparator	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-20):High Speed Comparator (PDF)	
	Low Power Comparator	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-21):Low Power Comparator (PDF)	
	OPAMP	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-22):Rail to rail OPAMP (PDF)	
	Analog Switch w/ Gate Voltage Booster	TSMC 40nm	Preliminary (Inquiry required)	IP_Datasheet(A-23):Analog Switch IP Core (PDF)	

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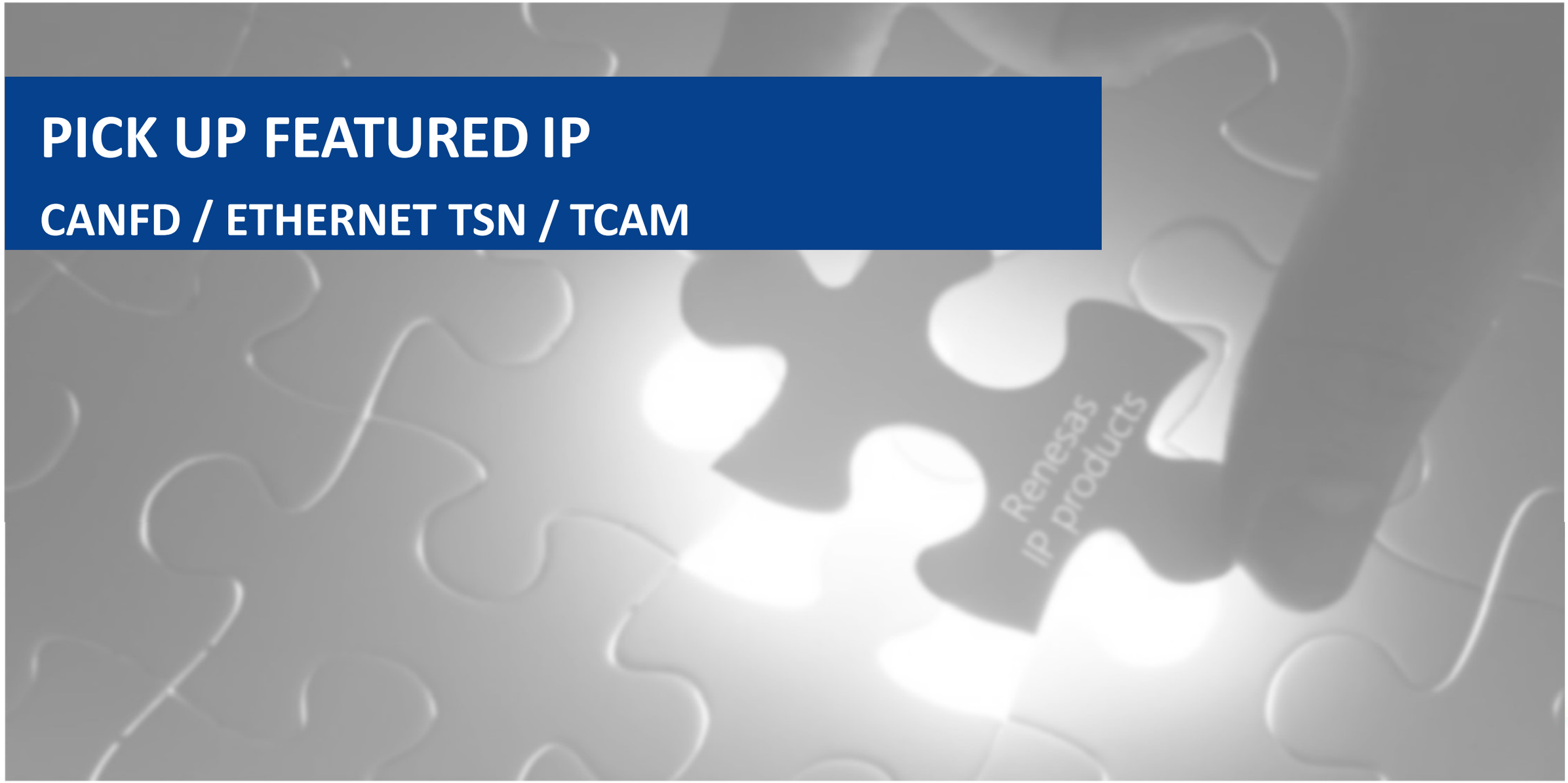
PICK UP FEATURED IP

CANFD / ETHERNET TSN / TCAM



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CAN / CAN FD IP PRODUCT LINEUP OVERVIEW

IP GROUP WITH SILICON PROVEN BY RENESAS DEVICES FOR AUTOMOTIVE APPLICATIONS

- Our CAN IP that has a track record of being installed in Automotive, General-purpose devices of Renesas Electronics
- ~~A new IP has been added~~ to the CAN controller IP, which has received many inquiries from automotive and industrial applications.
- By specializing in 1CH, the circuit scale has been reduced, contributing to cost reduction by small area on silicon.

Function	IP name	Process (or Soft macro)	Status	Document	Inquiry
CAN	CAN controller	Soft macro	Available	PDF	CONTACT
CAN FD	CAN FD controller	Soft macro	Available	PDF	
New CAN FD Lite	CAN FD controller	Soft macro	Available	PDF	

Overview specifications / features

New IP

Items	RCAN2	RS-CAN	RS-CAN Lite	RS-CANFD	RS-CANFD Lite
Standards	CAN2.0	CAN2.0	CAN2.0	CAN2.0/CAN-FD	CAN2.0/CAN-FD
CH #	1	6 (Fix)	1	2/4/6/8 (Selectable)	1
ID	32 ID	64 ID/CH	16 ID/CH	192 ID/CH	32 ID/CH
Receiver Buffer	32 buffers	384 buffers/6CH	16 buffers	2048 buffer/8CH	16 buffers
Transmitter Buffer		16 buffers/CH	4 buffers/CH	64 buffers/CH	4 buffers/CH
	・RX FIFO / TX FIFO	・RX FIFO / TX FIFO	・RX FIFO / TX FIFO	・RX FIFO / TX FIFO	・RX FIFO / TX FIFO
Features		・TXQ ・Multi-channel support ・Supports routing between CHs		・TXQ ・Multi-channel support ・Supports routing between CHs ・Payload filter	・TXQ ・Payload filter

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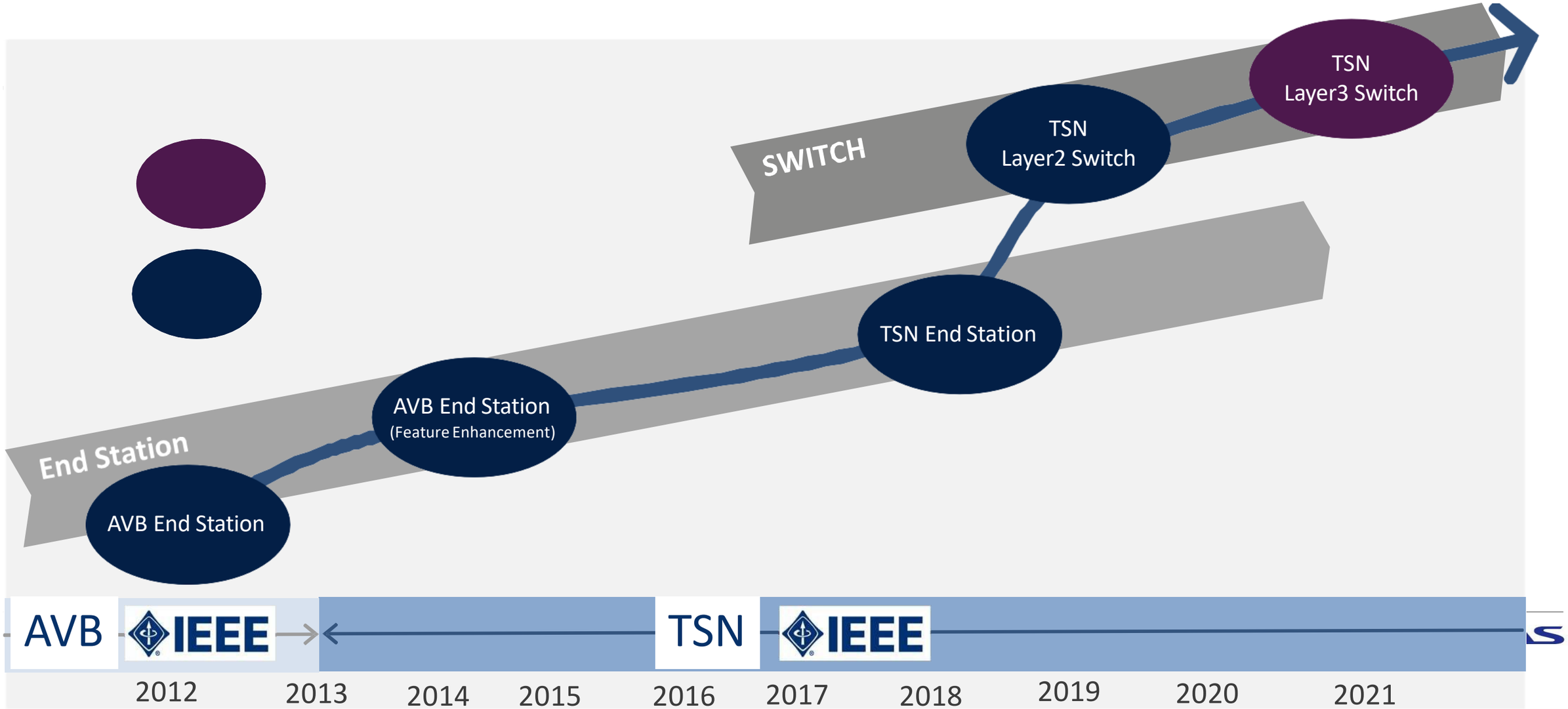
Renesas ETHERNET IP ROADMAP



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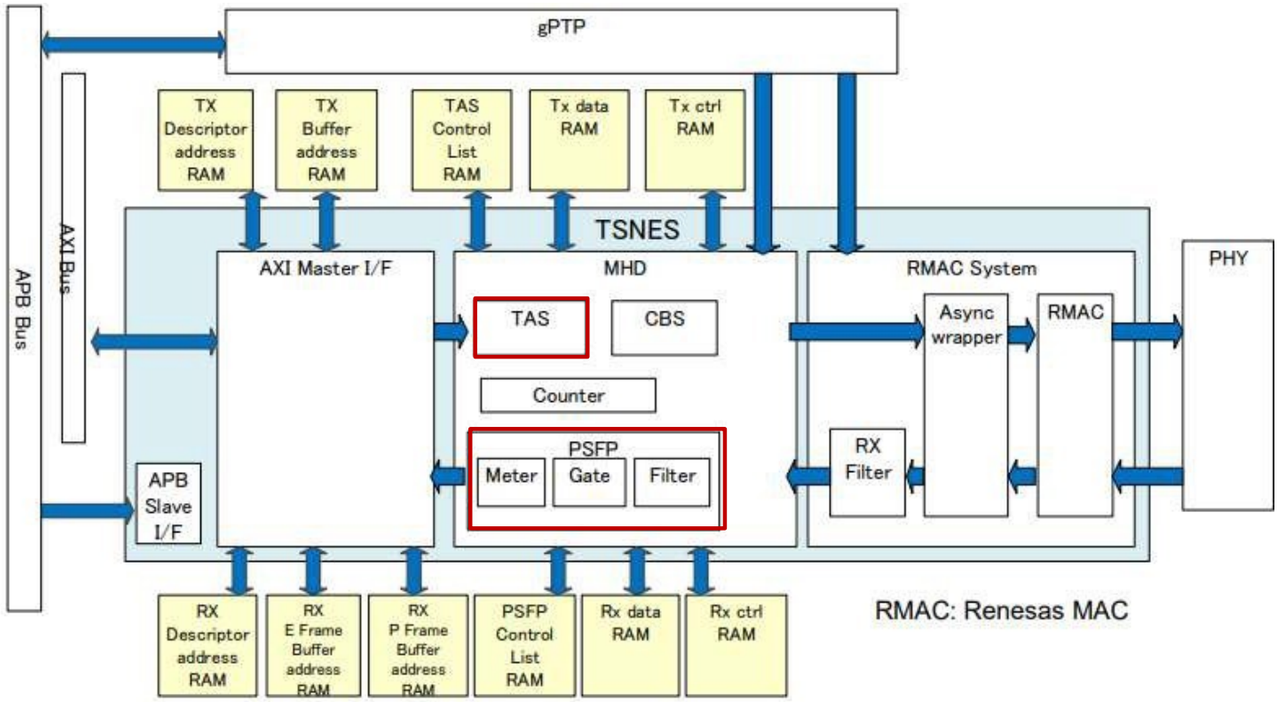
Ethernet TSN End Station
FOR TIME-SENSITIVE APPLICATIONS

Overview

- Including RMAC System compliant with IEEE802.3
- Support AXI/APB interface

Key Features

- 10/100/1000Mbps – full-duplex operation
- PHY Interface MII/RMII/GMII/RGMII/SGMII (RMII/RGMII/SGMII need protocol converter)
- Support Receive filtering (for L2~L4)
- Support various TSN standard



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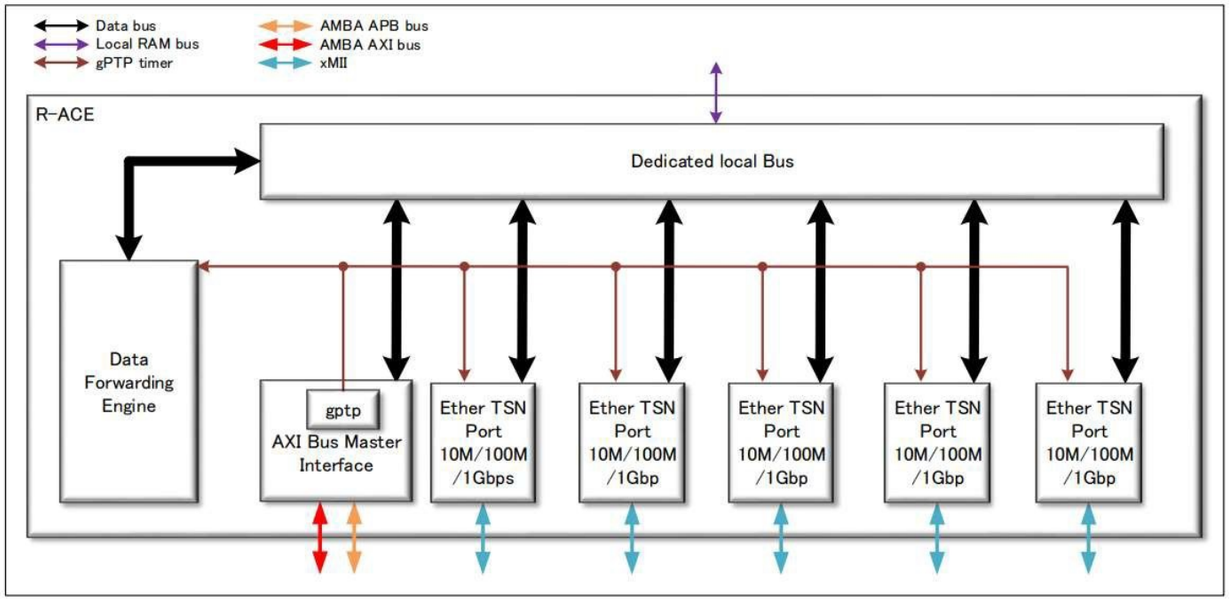
Ethernet TSN layer 2switch
FOR TIME-SENSITIVE APPLICATIONS

Overview

- 5Port Layer 2 Switch compatible with TSN standard
- Frame forwarding by exclusive bus

Key Features

- 10/100/1000Mbps – full-duplex operation
- PHY Interface MII/RMII/GMII/RGMII/SGMII (RMII/RGMII/SGMII need protocol converter)
- Support Receive filtering (for L2~L4)
- Support various TSN standard
- The number of ports and functions can be increased or decreased



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Feature of Renesas eTCAM IP

Embedded Ternary Content Addressable Memory IP

- **Providing Advanced TCAM technology based on wide development experience**

- Design oriented on Discrete TCAM Products
- Low Power and Small Area Design
- Silicon Evaluation based on TCAM mass production
- Configurable Wrapper RTL with Soft Priority Encoder
- BIST support

Less Power

- Valid Bit Control
- Search Key Mask

Smart Operation

- Quick Initialize Sequence
- RTL BIST Wrapper

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RENESAS e-TCAM 28nm/16nm/12nm/7nm

Embedded Ternary Content Addressable Memory IP

Feature of Renesas e-TCAM

Function

- One cycle operation latency (without priority encoder)
- Entry address / Bit width expansion can be supported by RTL Wrapper

Low Power

- Valid Bit per entry to reduce power
- Mask input option for bit-write and masked search key
- All Mismatch output and Pre-Search function support (from 7nm)

Cost Effective

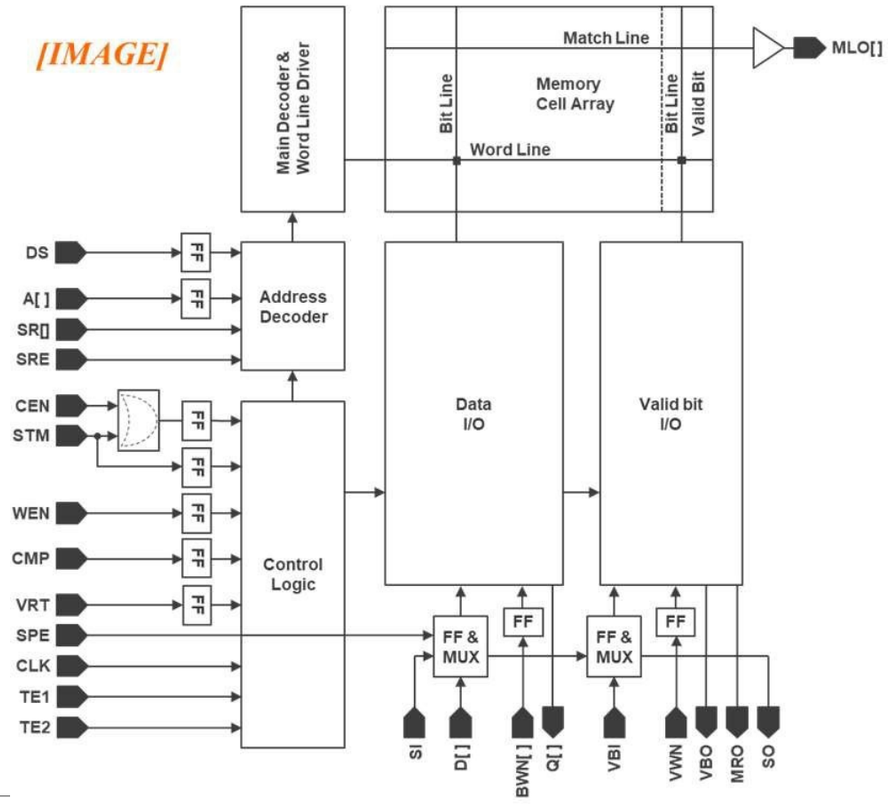
- BIST support with redundancy

Shorten TAT

- Additional power emulation library support

Technology Capabilities

Technology	Entry Address	Bit Width	Frequency
N28HPC / N28HPC+	128,256,512	4~40/step1	600MHz
N16FF / N16FFC	128,256	4~40/step1	950MHz
N12FFC	128,256	4~40/step1	1.1GHZ
N7	128,256	4~40/step1	1.3GHz



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Block Diagram for 28/16/12nm w/ Redundancy

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